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Practitioner's Docket No.: TSL-105

1AU 2814

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ishai Nachumovsky
Assignee: Tower Semiconductor Ltd.
Serial No.: 09/975,049-1005 Group No.: 2814
Filed: 10/10/2001 Examiner: Howard Weiss
For: "TWO-BIT-SPLIT-GATE NON-VOLATILE MEMORY TRANSISTOR"

#3
Election
FJONES
5-31-02

May 8, 2002

Commissioner of Patents and Trademarks
Box NON-FEE AMENDMENT
Washington, D.C. 20231

RESPONSE TO RESTRICTION REQUIREMENT

Sir:

In response to the outstanding Office Action dated April 30, 2002, in which the Examiner imposed a restriction requirement to election of invention for the above-referenced application, Applicant elects to prosecute the invention as in Group I, Claims 1-10 drawn to a semiconductor device, classified in Class 257, Subclass 314+, without traverse.

Applicant reserves the right to file divisional applications on the non-elected claims.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as FIRST CLASS MAIL in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C., 20231-0001, on May 8, 2002

Date: 5/8/2002 Signature: Carrie Reddick